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# Implementation of WATM-DLC protocols for a 34 MBit/s FDD Air Interface

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**Abstract:** This paper focuses on implementation issues concerning the Wireless ATM (W-ATM) protocols of the dynamic link control layer (DLC) for the demonstrator platform of the ACTS project SAMBA (System for Advanced Mobile Applications). Examples of the hardware architecture, the software design and implementation approaches are described for a protocol processing which has to cope with bit rates of up to 68 Mbit/s (34 Mbit/s simultaneously on up- and downlink).

## 1 Introduction.

Based on the research carried out in the R2067 MBS (Mobile Broadband System)[1,2] project the follow-up AC204 SAMBA (System for Advanced Mobile Application) project [3] focuses on building a trial platform and continues the system studies for future implementations. One of the key issues of the MBS concept is to give mobile users access to the services of the B-ISDN (Broadband Integrated Services Digital Network) while providing the same QoS (Quality of Service) as the fixed network does. Therefore a promising approach is to extend the stochastic multiplexing principle of the Asynchronous Transfer Mode (ATM) of the B-ISDN to the air interface. This paper briefly describes the applied DLC protocols developed for Wireless ATM (W-ATM) and, in more detail, their integration into a demonstrator platform. It focuses on the chosen approaches, methods and algorithms used for the real time implementation of these protocols with respect to the constraints and capabilities provided by the physical layer (modem) and the processing platform (Control Unit, CU) for protocol execution. Due to the user requirements the protocol processing has to provide user bit rates of up to 68 MBit/s (34 Mbit/s simultaneously on up- and downlink).

## 2 Architecture of the Control Unit

Providing flexible stochastic multiplexing at such high data rates makes protocol execution a task with a very high demand on processing power and strict real time requirements. Due to the tight time schedule of the SAMBA project a processing platform commercially available had to be chosen. The investigations of available products lead to the selection of powerPC based CPU boards, controlled by the multiple node real time operating system pSOS+M. While for the mobile terminal only one powerPC board is operated, the base station consists of three boards connected via VME bus. One board for each radio cell and the third board is used for the execution of the mobility management protocols, online monitoring and data sampling for performance evaluation. The CPU boards which execute the protocol stack including the DLC protocols and ATM layer functions are connected via the PCI bus with fast ACM (ATM cell memory) boards especially developed for this trial platform by Robert Bosch GmbH, Germany. Besides the connections to the BBPU (Base Band Processing Unit) interface and the Cellware ATM equipment, these boards provide fast memory to store ATM cell payload. With these concept extensive cell copying is

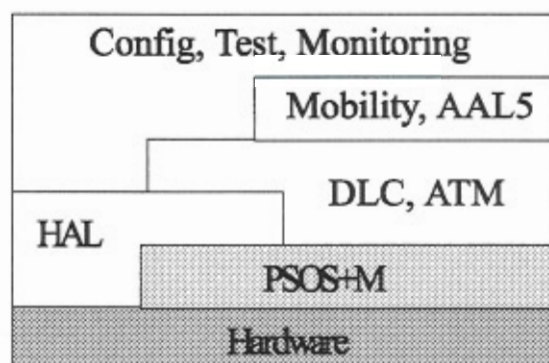


Figure 1: Layered Software Structure

The CPU boards which execute the protocol stack including the DLC protocols and ATM layer functions are connected via the PCI bus with fast ACM (ATM cell memory) boards especially developed for this trial platform by Robert Bosch GmbH, Germany. Besides the connections to the BBPU (Base Band Processing Unit) interface and the Cellware ATM equipment, these boards provide fast memory to store ATM cell payload. With these concept extensive cell copying is

avoided, as for protocol processing it is sufficient to consider the cell headers and some additional protocol control information. In addition to the ACM board an API (Application Programming Interface) called HAL (Hardware Abstraction Layer) is developed by Bosch, which makes the services of the physical layer available for the DLC software, see Figure 1.

### 3 The Software Implementation Approach of DLC and ATM layer

The protocols and algorithms applied in the DLC layer have been developed and evaluated in the past using an object oriented system simulation tool written in C++ and based on the CNCL (Communication Networks Class Library) [9], which provides an event driven simulation environment. The protocols, algorithms and utility functions have been implemented with respect to a flexible and versatile usage. The structure has been based on the OSI reference model to enable the fast and easy replacement of whole layers. The run time efficient execution of the protocols has been a second order optimisation criterion so far. For the implementation of the DLC protocols on the powerPC system the well structured approach of the simulator could only be used as a skeleton since the considered bit rates make fast and efficient protocol execution the main objective which prohibits the use of a strict OSI structure for the software.

Based on experiences gained so far, an object oriented approach for the design and implementation of communication protocols is the most promising solution. Hence also for the implementation on the powerPC system it was stuck to this approach and C++ was used. To overcome the drawback of C++, the excessive dynamic memory usage which is rather time consuming, the object management of the software has been based on a self developed memory management concept, which mostly avoids the dynamic allocation of system memory. The protocol execution consists of time critical data transmission routines and service routines with lower priority. The obvious approach to use two pSOS+M tasks with different priorities has been evaluated and discarded since the extensive task switching seemed to be too time consuming. Instead only one main task is used which is connected with an software interrupt service routine (ASR, Asynchronous Signal Routine). The ASR method avoids task switching and enables the interruption of the service routines by the more urgent data transmission functions. The interrupts which trigger the ASR are generated by the system hardware, e.g. the ACM board.

### 4 The DLC layer and ATM layer

One of the most challenging aspects of W-ATM is the extension of the stochastic multiplexing principle of ATM to the air interface. Therefore the protocol stack is extended by a DLC layer. The approach is to build a distributed ATM-multiplexer around the air interface which includes the base station, the wireless terminals and, most important, the radio channel. For the implementation of this distributed multiplexer, a medium access (MAC) protocol is needed that is able to perform stochastic multiplexing on the radio channel and that coordinates the access of the base station and the terminals to the shared radio resource. The virtual ATM connections operated by the terminals are controlled within the LLC layer, which also applies an adaptive ARQ (Automatic Repeat Request) protocol to enhance the reliability of the communication link [7,8].

#### 4.1 The Medium Access Control Layer (MAC)

The MAC layer executes the FDD (Frequency Division Duplexing) based version of the Dynamic Slot Assignment (DSA++) protocol family [4] with a fixed period length of 80 MAC-PDUs (Protocol Data Unit) [3]. The MAC-PDUs contain 2 ATM cells and an additional 32bit CI field (Control Information). A MAC connection (Data Channel, DCH) is established for each wireless terminal. A challenging aspect in the implementation of this MAC scheme are the influences of the processing delays. Simulation studies carried out with respect to real time implementation [5] have shown that an appropriate arrangement of signalling and data slots allows to cope with these delays, see Figure 2. The structure reflects the processing delay  $\tau_{eval}$  which is needed to evaluate MAC-PDUs received via the air interface. During  $\tau_{gen}$  received uplink signalling messages are decoded to be considered for the next downlink signalling message.



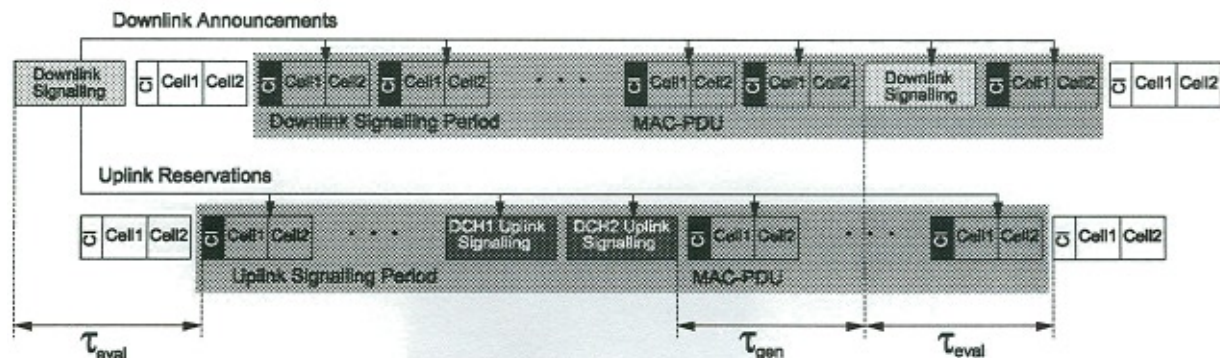


Figure 2: Structure of the DSA++ signalling period with processing delays

The flexible arrangement of signalling slots reduces the influence of the delays introduced by protocol processing. Figure 3 shows the usage of the control information field. The DCH Identifier (DCH Id) is a temporary valid short address for the mobile terminal which is assigned during the establishment of the MAC connection. BSC Id and BST Id are used to identify the corresponding base station controller and base station transceiver (architecture details can be found in [3]). The type field describes the content of the cell fields (MAC command PDUs, LLC command PDUs, ATM cells or empty). The urgent bit indicates a message with higher priority. This is used for a preferred processing of the downlink signalling message. The signalling type field determines the usage of the signalling information field. On the downlink only LLC-acknowledgements are transmitted. On the uplink the LLC-acknowledgements compete with the transmission of capacity request messages (dynamic parameters). These dynamic parameters are different for each service class, see Figure 3. *NIL Dynamic Parameters* is sent if no more capacity is requested. The dynamic parameters for the CBR service class are mainly used for synchronisation, since the deterministic arrival times of CBR cells is exploited. However, the optimised handling of CBR connections is not implemented in the demonstrator platform. Capacity requests for CBR connections also use the *VBR Dynamic Parameters*. The LLC acknowledgement consists of a type field which determines the type of the acknowledgement (Receive Ready, Selective Reject or Reject), an ARQ Id used as a short address and sequence number which indicates, the expected PDU or the missing PDU respectively.

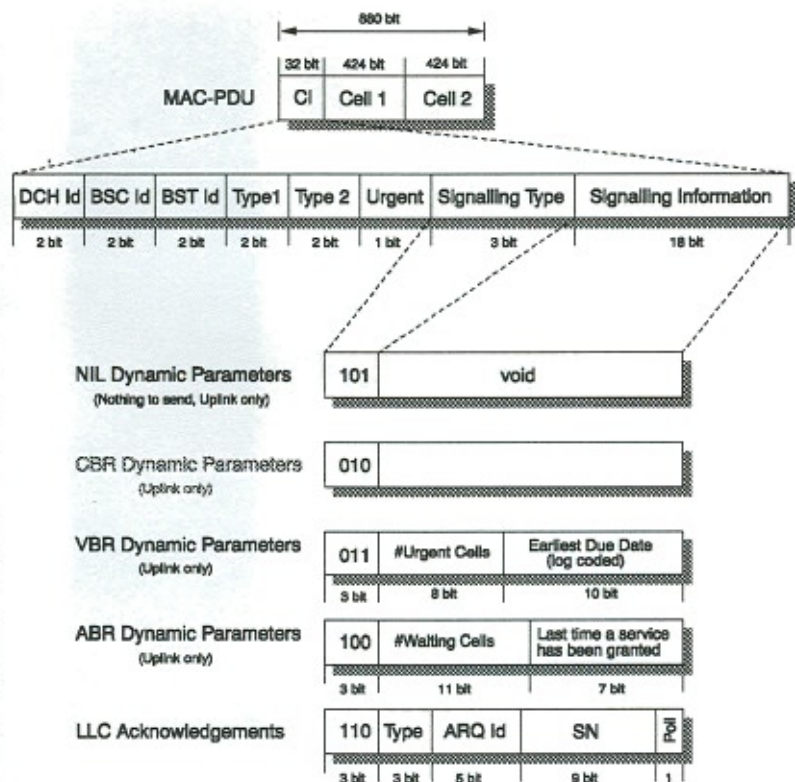


Figure 3: Usage of control information (CI) field

## 4.2 The Logical Link Control Layer (LLC)

The LLC layer contains the ARQ-instances which perform the error recovery and connection management functions. The functions within the LLC layers are based on the processing of single ATM cells and additional protocol control information (sequence number, ARQ identifier and a poll bit). The VCI (Virtual channel identifier) and the VPI (virtual path identifier) are mapped by the LLC layer to an ARQ-Identifier (ARQ Id). The ARQ-Id is used as a short address and reduces the signalling overhead especially for the transmissions of acknowledgements. The LLC layer contains an ARQ-manager, which performs the multiplexing of the active virtual channels to the appropriate DCH, an ARQ-instance object which contains the ARQ-sender and the ARQ-receiver and ARQ-evaluation objects which determine the performance figures such as cell loss, delay and throughput for scientific evaluation of the system. The DLC-manager contains the interface to the functions of the MAC and ATM layer.

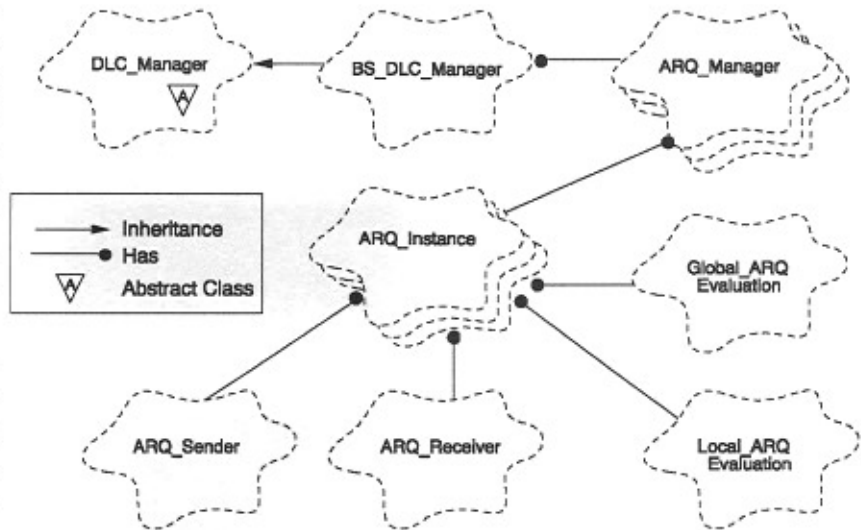


Figure 4: C++ Object Structure of basestation LLC layer [6]

## 4.3 The ATM layer

The ATM layer relies on the services of the DLC layer and has to communicate with the mobility management protocols. Since these functions are distributed to three processor boards in the basestation, the ATM layer organises the communication between the nodes and provides a common interface for the higher layers to the protocol functions. Therefore service primitives and control procedures have been developed to enable the common access to the distributed functions within the ATM layer using shared memory communication via the VME bus.

## 5 Handover

One of the objectives of the SAMBA project is to provide a seamless radio handover when the mobile terminal changes from one radio cell to the other. Since a separate ACM board and a dedicated CPU board are assigned to each BST (Base Station Transceiver), all stored ATM cells as well as additional LLC protocol information have to be exchanged between the two nodes in case of handover. This is a rather time consuming tasks, which causes the development of buffering techniques and three different handover procedures that minimise the amount of data to be exchanged and cope with the hardware restrictions.

**Seamless backward handover:** The old radio link is still available and can be used to reduce the number of queued ATM cells which means that less cells have to be copied to the new BST.

**Seamless forward handover:** If the link quality is not sufficient to perform a backward handover a forward handover will be executed. All queued ATM cells have to be copied via the VME bus.

**Non-seamless forward handover:** Too many cells have been queued and cannot be copied due to hardware restrictions. They will be discarded which leads to a non seamless handover procedure.



## 6 Development approach and used tools

Due to the tight time schedule of the SAMBA project software development had to be performed in parallel to the hardware development. At the beginning only the powerPC boards and the operating sys-

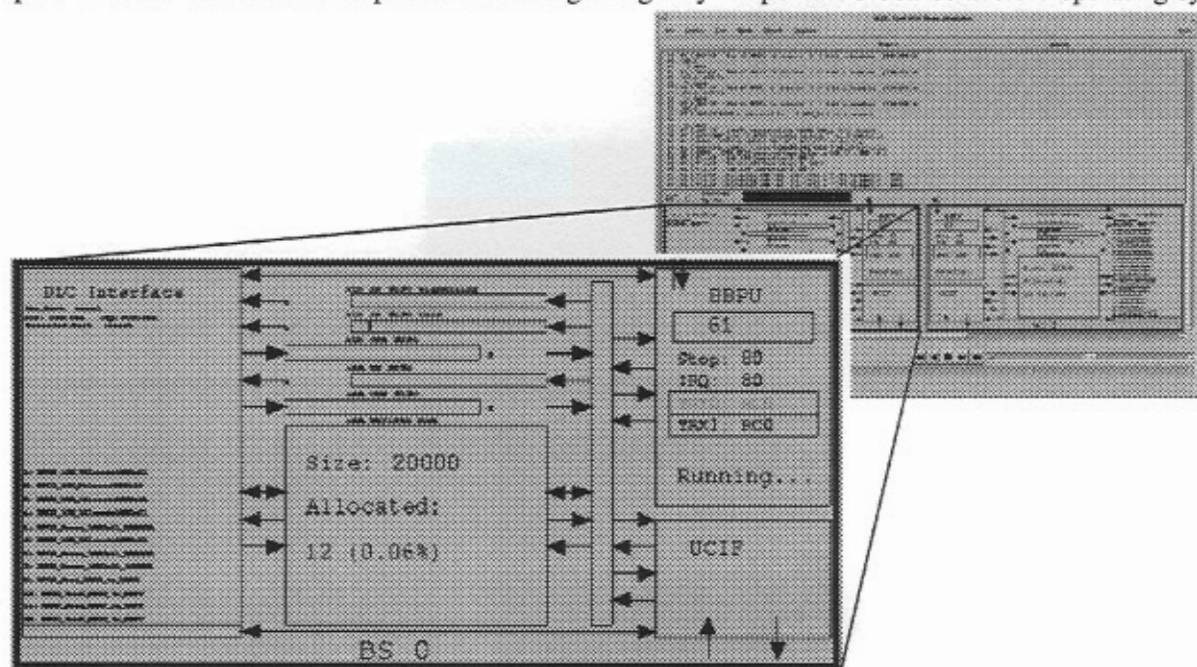


Figure 5: Screenshot of the ACM board emulation tool

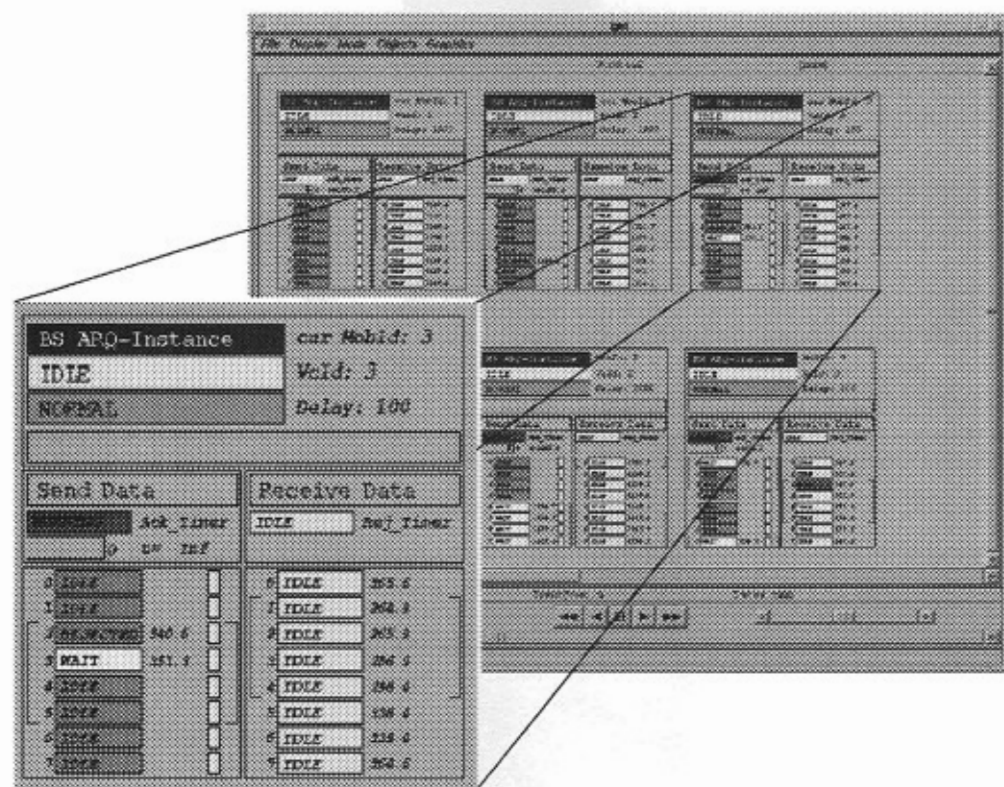


Figure 6: Screenshot of the LLC protocol debugging tool

tem were available for the software development. Therefore software emulations of key hardware components, mainly the ACM board and the BBPU, have been developed after the specification of the HAL interface. These emulations, which run on workstations, are based on the CNCL and use IP sockets for

the communication with the other system parts. Since many people were involved in the implementation and only three target system boards were available, a two pass development scheme was applied.

The first implementation step and the first function tests took place on workstations, considering the special features of the target hardware. After cross compiling the code for the powerPC system, in the second step function test of the protocols took place using the self developed system emulation and graphical protocol debugging tools. After the correct implementation of the protocols had been verified, a first integration step leads to a back to back link via the ACM boards of two CPU boards.

Figure 5 shows a screenshot of the ACM board emulation tool. The right part of the diagram shows the status of the I/O interfaces to the baseband processing unit (BBPU) and the fixed ATM network via the universal Cellware interface (UCIF). In the middle the state of the ATM payload RAM and the connecting FIFO memories is displayed. The right shows the messages sent to the DLC layer.

A screenshot from the LLC-protocol debugging tool is given in Figure 6. It shows states of sending and receiving windows for each virtual connection. As an example a selective repeat ARQ protocol with a maximum windows size of 4 is given. In the diagram PDU(2) has been rejected and PDU(3) has been sent but not yet acknowledged. Besides the state boxes the expiring dates of the PDUs is displayed, since a real time connection with a maximum cell transfer delay (CTD) of 100 slots is operated. In the upper part the state of the virtual connection, the queue length and protocol timers are depicted.

## 7 Acknowledgement

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